Combined PEALD gate-dielectric and *in-situ* SiN cap-layer for reduced V_{th} shift and $R_{DS\text{-}ON}$ dispersion of AlGaN/GaN HEMTs on 200 mm Si wafer

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Abstract

The present work focuses on the gate dielectric and MOCVD (MetalOrganic Chemical Vapour Deposition) capping layer of AlGaN/GaN transistors grown on 200 mm Si wafers. Firstly, it will be shown how a SiN gate dielectric grown by means of PEALD (Plasma Enhanced Atomic Layer Deposition) reduces the threshold voltage (V_{th}) shift induced by negative gate bias and the gate leakage with respect to a SiN gate dielectric grown by RTCVD (Rapid Thermal Chemical Vapor Deposition). Secondly, the dynamic $R_{DS\text{-}ON}$ dispersion of two samples with same gate dielectric (PEALD-SiN) but different MOCVD capping layer is compared. Results will show that the traps causing the $R_{DS\text{-}ON}$ dispersion are mainly located at the surface and that their amount can drastically be reduced by using *in-situ* MOCVD SiN as capping layer.

1. Introduction

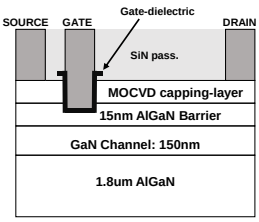
The use of GaN as substitute of Si for power-switching applications has raised several challenges to make this new technology competitive in terms of performances and costs. AlGaN/GaN HEMTs (High Electron Mobility Transistors) realized on 200 mm Si wafers with Au-free contacts (compatible with standard CMOS technology) seems today an attractive path to follow to reach a cost-effective high-performant device [1].

One of the main issues is the choice of the surface termination in the gate region to reduce both gate leakage and density of trap states at the semiconductor/passivation interface. The MISHEMT structure (Metal Insulator Semiconductor HEMT) is the best solution to suppress the gate leakage in both forward and reverse bias in comparison with a Schottky gate contact. In this paper we will compare two different techniques for the deposition of SiN as gate dielectric. One of the possibilities is the deposition by means of RTCVD. The characteristic of this technique is that the wafer is processed at high temperature for a short time [2]. The other possibility which will be analyzed is the deposition by means of PEALD. This process allows lower deposition temperature during the process, with lower density of interface states [3].

Several publications show how the surface treatment in the access regions improves the frequency response of the device (low dynamic $R_{DS\text{-}ON}$ dispersion) [4]. We will demonstrate a reduction of the dynamic $R_{DS\text{-}ON}$ dispersion by using an *in-situ* MOCVD SiN capping layer in the access region in a device with a PEALD SiN gate dielectric.

2. Experimental Details and Results

The first phase of the work focused on the study of the gate dielectric. For this purpose two wafers with identical epitaxial layers but different gate dielectrics were processed. The samples were grown on 200 mm <111> Si wafers. The top layers of the epi-stack consist of a 1.8 µm AlGaN buffer layer (8% Al content), a 150 nm GaN channel, a 15 nm $Al_{0.25}Ga_{0.75}N$ barrier and a 3 nm GaN-cap layer. The surface was passivated with SiN deposited by means of RTCVD. Then the gate region was etched to leave 3.7 nm AlGaN and form the gate recess. For the gate dielectric, a 15 nm layer of SiN was deposited by means of RTCVD at 700ºC on the first wafer. On the second wafer 15 nm SiN was deposited by means of PEALD in a "ASM Eagle® 12" deposition tool. Au-free metal contacts were used. A schematic cross-section of the device is reported in Fig.1 (wafers "A" and "B"). The devices measured had gate-drain distance L_{GD} = 5 µm, gate width W_{GD} = 100 or 200 µm, gate length L_G = 1.5 µm, gate-source distance L_{GS} = 0.75



	MOCVD capping-layer	Gate-dielectric
wafer A	3nm GaN	15 nm RTCVD SiN
wafer B	3nm GaN	15 nm PEALD SiN
wafer C	3nm GaN	25 nm PEALD SiN
wafer D	5nm in-situ SiN	25 nm PEALD SiN

Fig. 1 Schematic cross-section of the samples used in this work. The table shows the process splits: wafers "A" and "B" were used for the 1st experiment (V_{th} shift); wafers "C" and "D" were used for the 2nd experiment ($R_{DS\text{-}ON}$ dispersion).

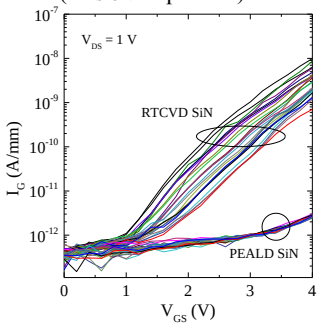


Fig. 2 Forward gate leakage of samples with RTCVD SiN as gate dielectric (wafer A) and samples with PEALD SiN as gate dielectric (wafer B).

µm, a gate field-plate and two levels of source field-plate (extending respectively 1 µm, 2 µm and 3 µm beyond the drain edge of the gate). On these devices leakage measurements and pulse I_D-V_{GS} measurements were performed. The gate leakage in forward bias is reported in Fig. 2. Devices with PEALD SiN gate dielectric have lower gate leakage compared to the devices with RTCVD SiN gate dielectric. Pulsed I_{DS}-V_{GS} measurements were performed by pulsing the device from a quiescent state (V_{GS_q}, V_{DS_q}) to a non-quiescent state (V_{GS_nq}, V_{DS_nq}). The frequency and the duty-cycle of the signal were f = 10 kHz and δ = 10%, respectively. The test equipment was an AURIGA AU4850. The same bias conditions were used to test both the RTCVD and the PEALD gate-dielectric samples. Example I_D-V_{GS} are reported in Fig. 3. The V_{th} is calculated as the intercept on the x axis of the linear interpolation of the I_D-V_{GS} at maximum g_m. The V_{th} shifts (ΔV_{th}) are summarized in Fig. 4. The samples with PEALD SiN have lower V_{th} shifts than the ones with RTCVD SiN.

Once the process for the gate dielectric was established, our attention moved to improve the dynamic $R_{DS\text{-}ON}$ by improving the surface quality on the access region of the device. With this purpose in mind two other wafers were processed with the same epi-stack shown in Fig. 1. A split was introduced on the last layer: in one of the two wafers the 3 nm GaN-cap layer was substituted by a 5 nm *in-situ* SiN-cap layer (wafers "C" and "D" in Fig. 1). Both wafers were then passivated by RTCVD SiN as *ex-situ* passivation layer. The gate dielectric was 25 nm PEALD SiN; note that with this thicker gate dielectric a smaller ΔV_{TH} and a lower gate leakage was found compared to the wafer with 15 nm PEALD SiN reported above. Pulsed I_D-V_{DS} measurements were performed with the same switching conditions as used for the I_D-V_{GS}. The V_{DS_q} was swept from 0 V to 198 V in 33 V steps, while the V_{GS_q} was kept constant. A comparison between a device with GaN-cap layer and one with *in-situ* SiN-cap layer is reported in Fig. 5. The I_D of the device with GaN-cap layer drops; whereas the I_D of the device with *in-situ* SiN-cap layer remains high up to pulsing from 198 V quiescent bias condition. To quantitatively evaluate the current collapse the dynamic $R_{DS\text{-}ON}$ was calculated from the slope of the I_D-V_{DS} in the linear region. Results are reported in Fig. 6. The average increase of the $R_{DS\text{-}ON}$ for the samples with *in-situ* SiN is 50%, moreover devices have a good uniformity over the wafer. On the other hand samples with GaN cap show an increase of $R_{DS\text{-}ON}$ that varies from 50% in the best case up to 10 times the initial value in the worst case, with low uniformity over the wafer. We conclude that the *in-situ* SiN-cap gives a better and more uniform passivation of the surface trap states in the gate-to-drain access region.

3. Conclusions

In this work gate leakage and dynamic *I-V* measurements were used to compare different gate dielectrics and different MOCVD cap-layers. It has been shown that PEALD SiN as gate dielectric gives better performance in terms of leakage and threshold voltage shift. It has also been shown that the *in-situ* deposited SiN cap-layer on the access region improves the dynamic response of the device with PEALD SiN gate dielectric.

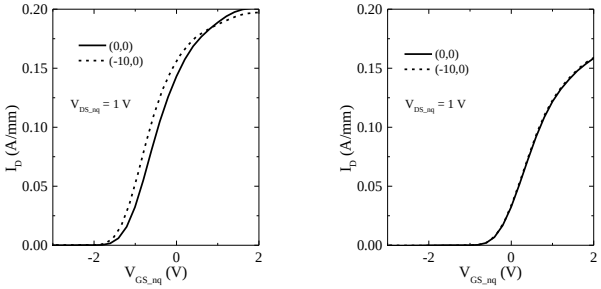


Fig. 3 Pulsed I_D-V_{GS} characteristics for a device with 15 nm RTCVD SiN gate-dielectric (left, wafer A) and a 15 nm PEALD SiN gate dielectric (right, wafer B).

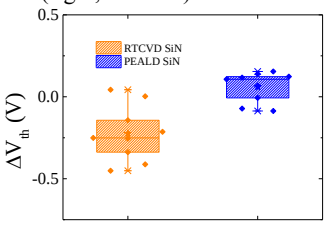


Fig. 4 Shift of the threshold voltage from the pulsed I_D-V_{GS} measurements. ΔV_{th} is calculated as $V_{th(-10,0)}$–$V_{th(0,0)}$

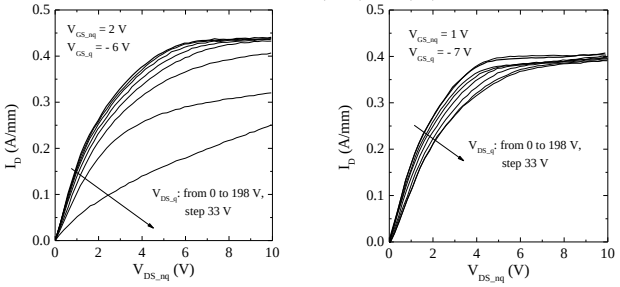


Fig. 5 Pulsed I_D-V_{DS} characteristics at different drain quiescent biases (V_{DS_q}). On the left: wafer C - sample with 25 nm PEALD SiN gate dielectric and GaN cap; on the right: wafer D - sample with 25 nm PEALD SiN gate dielectric and *in-situ* SiN cap.

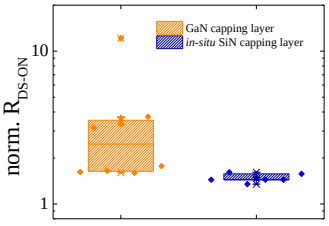


Fig. 6 Normalized $R_{DS\text{-}ON}$ measured pulsing from V_{DS_q} = 198 V quiescent bias condition.

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